CLAIMS

What is claimed is:

1. A calibrated digital-to-analog converter (DAC), comprising:

a main DAC having a digital input and an analog output, the main DAC being configured, in the event a plurality of first digital code values are applied to its digital input, to produce corresponding analog output values at its analog output, wherein the analog output values produced by the main DAC deviate from desired analog output values of the main DAC;

a memory having an address input and first and second data outputs, the memory being configured to store a plurality of second digital code values representing respective digital correction values, the memory being configured, in the event a predetermined number of high order bits of the first digital code values are applied to its address input, to provide selected consecutive correction values at its first and second data outputs, respectively;

a first calibration DAC having a digital input, an analog output, a positive reference (Vref+) voltage input, and a negative reference (Vref-) voltage input, the first calibration DAC being configured, in the event Vref+ and Vref- voltage levels corresponding to the consecutive correction values provided at the first and second data outputs, respectively, of the memory are applied to its Vref+ and Vref- voltage inputs, and a sequence of low order bits of the first digital code values is applied to its

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

digital input, to produce corresponding analog output values at its analog output; and

an analog summing circuit configured to receive the analog outputs produced by the main DAC and the first calibration DAC, and to subtract the analog output of the first calibration DAC from the analog output of the main DAC to generate a calibrated analog output.

2. The calibrated DAC of claim 1 further including second and third calibration DACs having respective digital inputs and respective analog outputs, the second and third calibration DACs being configured, in the event the consecutive correction values provided at the first and second data outputs, respectively, of the memory are applied to their respective digital inputs, to produce corresponding analog output values at their respective analog outputs representing the Vref+ and Vref- voltage levels.

3. The calibrated DAC of claim 2 wherein the second calibration DAC is configured to provide the Vref+ voltage level to the Vref+ voltage input of the first calibration DAC, and wherein the third calibration DAC is configured to provide the Vref- voltage level to the Vref- voltage input of the first calibration DAC.

4. The calibrated DAC of claim 1 wherein the first calibration DAC is further configured to interpolate between the Vref+ and Vref- voltage levels, thereby producing a piecewise linear approximation of an integral non-linearity error curve of the main DAC.

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

5. The calibrated DAC of claim 4 wherein the consecutive correction values correspond to consecutive piecewise linear breakpoint code values of the piecewise linear approximation.

6. The calibrated DAC of claim 5 wherein the piecewise linear breakpoint code values are substantially equally spaced within the piecewise linear approximation.

7. The calibrated DAC of claim 4 wherein the first calibration DAC is further configured to interpolate from the Vref- voltage level to the Vref+ voltage level, or from the Vref+ voltage level to the Vref- voltage level, based at least in part on the relative magnitudes of the consecutive correction values.

8. The calibrated DAC of claim 1 wherein the memory comprises a nonvolatile memory circuit.

9. The calibrated DAC of claim 8 wherein the memory circuit is selected from the group consisting of a fuse link memory, an EEPROM, and a FLASH memory.

10. The calibrated DAC of claim 1 wherein the main DAC has a resistor string architecture.

11. The calibrated DAC of claim 1 wherein the first calibration DAC has an R-2R type binary architecture.

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

12. The calibrated DAC of claim 2 wherein each one of the first, second, and third calibration DACs has an R-2R type binary architecture.

13. The calibrated DAC of claim 1 wherein the selected consecutive correction values provided first by the memory at its respective data outputs are used to correct an offset error of the analog output.

14. The calibrated DAC of claim 1 wherein the selected consecutive correction values provided last by the memory at its respective data outputs are used to correct a full-scale error of the analog output.

15. The calibrated DAC of claim 1 wherein the memory comprises a volatile memory circuit.

16. The calibrated DAC of claim 15 wherein the memory is configured to receive the respective digital correction values downloaded via a digital interface.

17. The calibrated DAC of claim 1 wherein the main DAC, the memory, the first calibration DAC, and the analog summing circuit are implemented on an integrated circuit.

18. The calibrated DAC of claim 1 wherein the main DAC, the first calibration DAC, and the analog summing circuit are implemented on an integrated circuit, and the memory is implemented external to the integrated circuit.

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

19. A method of calibrating a digital-to-analog converter (DAC), comprising the steps of:

providing a main DAC having a digital input and an analog output;

in the event a plurality of first digital code values are applied to the digital input of the main DAC, producing corresponding analog output values at the analog output of the main DAC, wherein the analog output values produced by the main DAC deviate from desired analog output values of the main DAC;

storing a plurality of second digital code values representing respective digital correction values within a memory;

in the event a predetermined number of high order bits of the first digital code values are applied to an address input of the memory, providing selected consecutive correction values at first and second data outputs of the memory, respectively;

providing a first calibration DAC having a digital input, an analog output, a positive reference (Vref+) voltage input, and a negative reference (Vref-) voltage input;

in the event Vref+ and Vref- voltage levels corresponding to the consecutive correction values provided at the first and second data outputs, respectively, of the memory are applied to the Vref+ and Vref- voltage inputs of the first calibration DAC, and a sequence of low order bits of the first digital code values is applied to the digital input of the first calibration DAC, producing corresponding

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

analog output values at the analog output of the first calibration DAC;

receiving the analog outputs produced by the main DAC and the first calibration DAC by an analog summing circuit; and

subtracting the analog output of the first calibration DAC from the analog output of the main DAC by the analog summing circuit to generate a calibrated analog output.

20. The method of claim 19 further including the steps of

providing second and third calibration DACs having respective digital inputs and respective analog outputs, and

in the event the consecutive correction values provided at the first and second data outputs, respectively, of the memory are applied to the respective digital inputs of the second and third calibration DACs, producing corresponding analog output values at the respective analog outputs of the second and third calibration DACs, the corresponding analog output values representing the Vref+ and Vref- voltage levels.

21. The method of claim 20 further including the steps of providing the Vref+ voltage level to the Vref+ voltage input of the first calibration DAC by the second calibration DAC, and providing the Vref- voltage level to the Vref- voltage input of the first calibration DAC by the third calibration DAC.

22. The method of claim 19 wherein the selected consecutive correction values provided first in the second providing

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

step are used to correct an offset error of the analog output.

23. The method of claim 19 wherein the selected consecutive correction values provided last in the second providing step are used to correct a full-scale error of the analog output.

24. The method of claim 19 further including the step of downloading the respective digital correction values to the memory.

25. The method of claim 24 wherein the memory comprises a volatile memory circuit.

26. The method of claim 19 wherein the main DAC, the memory, the first calibration DAC, and the analog summing circuit are implemented on an integrated circuit.

27. The method of claim 19 wherein the main DAC, the first calibration DAC, and the analog summing circuit are implemented on an integrated circuit, and the memory is implemented external to the integrated circuit.

ATTORNEY DOCKET NO. TI-36338 (UNITI-177XX)
WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313